PROGRAMMABLE ERROR CHECKING VALUE CIRCUIT AND METHOD

ABSTRACT OF THE DISCLOSURE

An arbiter system comprises a plurality of hardware resources, a common resource, and an arbiter. The plurality of hardware resources are divided into groups of hardware resources and are coupled to the common resource and the arbiter. The arbiter controls which of the plurality of hardware resources has priority to access to the common resource. The arbiter includes a group shifting arbiter which shifts priority among the groups of hardware resources and a level shifting arbiter which separately shifts priority among the hardware resources within each of the groups. An error checking value generator system comprises a general purpose DMA controller and an arithmetic circuit. The arithmetic circuit is coupled to receive data from the general purpose DMA controller. The arithmetic circuit generates an error checking value based on the data received from the general purpose DMA controller and based on a polynomial equation. The arithmetic circuit is capable of being programmed with a plurality of different polynomial equations usable to generate error checking values of different types.